Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 10, 21 and 26, as follows:

Listing of Claims:

1. (Currently Amended) A memory module comprising;

a circuit board;

a memory hub positioned on the circuit board;

a plurality of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, and the first end of each memory device in each pair being positioned adjacent one another on the circuit board and the second end of each device in a pair being positioned adjacent a second end of a device in one of the other pairs; ~~and~~

a plurality of command-address busses, each command-address bus coupled to the memory hub and at least two memory devices, the two memory devices being from a different pair; and

an edge connector positioned along an edge of the circuit board and coupled to the memory hub.

2. (Original) The memory module of claim 1 wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals.

3. (Previously Presented) The memory module of claim 1 wherein the memory devices comprise dynamic random access memories.

4. (Original) The memory module of claim 1 further comprising a second edge connector positioned along a second edge of the circuit board and coupled to the memory hub.

5. (Original) The memory module of claim 1 wherein the module includes four pairs of devices, each pair being positioned adjacent a respective edge of the circuit board, and wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals.

6. (Previously Presented) The memory module of claim 5 wherein the data signals of each memory device are carried on a data bus which is 9-bits wide.

7. (Original) The memory module of claim 1 wherein the module includes eight pairs of memory devices, four pairs positioned on a front side of the circuit board and four pairs positioned on a back side of the circuit board, each pair on the front side being positioned adjacent a corresponding pair on the back side, and wherein the eight pairs of memory devices comprise a single rank on the memory module.

8. (Previously Presented) The memory module of claim 7 wherein each of the memory devices includes a data bus, and wherein the data bus of half the memory devices are 4-bits wide and the data bus of the other half of the memory devices are 5 bits wide.

9. (Original) The memory module of claim 1 wherein the plurality of memory devices positioned around the memory hub are positioned on a front side of the circuit board, and wherein the memory module further comprises a second rank of memory devices positioned on a back side of the circuit board, each device on the back side being positioned adjacent a corresponding device on the front side.

10. (Currently Amended) A memory module comprising;

a circuit board;

a memory hub positioned on the circuit board;

a plurality of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout without pins or leads extending beyond an outer perimeter of each respective memory device and where the pin layout includes ~~including~~ pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, and the first end of each memory device in each pair being positioned abutting one another on the circuit board; and

an edge connector positioned along an edge of the circuit board and coupled to the memory hub.

11. (Original) The memory module of claim 10 wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals.

12. (Previously Presented) The memory module of claim 10 wherein the memory devices comprise dynamic random access memories.

13. (Original) The memory module of claim 10 further comprising a second edge connector positioned along a second edge of the circuit board and coupled to the memory hub.

14. (Previously Presented) The memory module of claim 10 wherein the module includes four pairs of devices, each pair being positioned perpendicular to adjacent pairs and located adjacent a respective edge of the circuit board, and wherein the first functional group

of signals comprise data signals and the second functional group of signals comprise control-address signals.

15. (Previously Presented) The memory module of claim 14 wherein the data signals of each memory device are carried on a data bus which is 9-bits wide.

16. (Previously Presented) The memory module of claim 11 wherein the module includes a first pair of memory devices positioned adjacent a respective edge of the circuit board and a second pair positioned adjacent a diagonal opposite edge of the circuit board.

17. (Previously Presented) The memory module of claim 16 wherein the data signals of each memory device are carried on a data bus which is 18-bits wide.

18. (Original) The memory module of claim 10 wherein the module includes eight pairs of memory devices, four pairs positioned on a front side of the circuit board and four pairs positioned on a back side of the circuit board, each pair on the front side being positioned adjacent a corresponding pair on the back side, and wherein the eight pairs of memory devices comprise a single rank on the memory module.

19. (Previously Presented) The memory module of claim 18 wherein each of the memory devices includes a data bus, and wherein the data bus of half the memory devices are 4-bits wide and the data bus of the other half of the memory devices are 5 bits wide.

20. (Original) The memory module of claim 10 wherein the plurality of memory devices positioned around the memory hub are positioned on a front side of the circuit board, and wherein the memory module further comprises a second rank of memory devices positioned on a back side of the circuit board, each device on the back side being positioned adjacent a corresponding device on the front side.

21. (Currently Amended) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and data output devices;

a controller electrically coupled to the processor, the controller being operable to receive and transmit memory signals on a high-speed data link;

at least one memory module coupled to the controller, each memory module comprising:

a circuit board;

a memory hub positioned on the circuit board;

a plurality of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, and the first ends of each memory device in each pair abutting one another on the circuit board; ~~and~~

a plurality of command-address busses, each command-address bus coupled to the memory hub and at least two memory devices, the two memory devices being from a different pair; and

an edge connector positioned along an edge of the circuit board and coupled to the memory hub.

22. (Previously Presented) The computer system of claim 21 wherein the memory devices comprise dynamic random access memories.

23. (Original) The computer system of claim 21 wherein the memory modules are coupled in a daisy chain manner to the controller.

24. (Original) The computer system of claim 21 wherein the high-speed data link comprises an optical communications link.

25. (Original) The computer system of claim 21 wherein on each memory module the plurality of memory devices positioned around the memory hub are positioned on a front side of the circuit board, and wherein the memory module further comprises a second rank of memory devices positioned on a back side of the circuit board, each device on the back side being positioned adjacent a corresponding device on the front side.

26. (Currently Amended) A method of forming a memory module including a circuit board, the method comprising:

positioning a memory hub on the circuit board;

positioning pairs of memory devices around the memory hub such that both devices in each pair are on the same side of the circuit board and each pair is perpendicular to adjacent pairs, each memory device in a respective pair being physically rotated 180 degrees in the plane of the circuit board relative to the other device in the pair;

coupling data signals between the memory hub and each memory device;

coupling control-address signals between the memory hub and two memory devices via a common path, the two memory devices being from different pairs; and

~~coupling data and control address signals between the memory devices and the hub; and~~

routing a system bus to the memory hub.

27. (Previously Presented) The method of claim 26 wherein each memory device includes a pin 1 designated end and a first functional group of signals are adjacent this end of the device, and wherein the devices in each pair are positioned with the pin 1 designated ends abutting one another.

28. (Original) The method of claim 27 wherein the first functional group of signals comprises data bus signals.

29. (Previously Presented) The method of claim 26 wherein a data bus is routed between the hub and each device, and wherein signal lines of the data bus are routed parallel to edges of the circuit board.

30. (Original) The method of claim 26 wherein a control-address bus is routed between the hub and one device in each pair, and wherein signal lines of the control-address bus are routed diagonally outward from the hub towards corners of the circuit board.